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(54) Apparatus for Remotely Reading Data Storage Devices

(57) The apparatus allows the reading of data from a number of data storage devices (e.g. tags, IC cards) designed to communicate data to a corresponding compatible reader in response to an interrogation signal and using a carrier modulation and data transmission system designed for that data storage device and corresponding reader. An antenna (26) is provided to transmit a signal to and receive a response from the data storage device (1). Signal processors (DSP 1 and DSP 2) are used in combination with a microprocessor (21) to identify the carrier modulation and data transmission system from characteristic features thereof and then to analyze the response signal in accordance with the identified carrier modulation and data transmission system to determine the data stored by the data storage device.

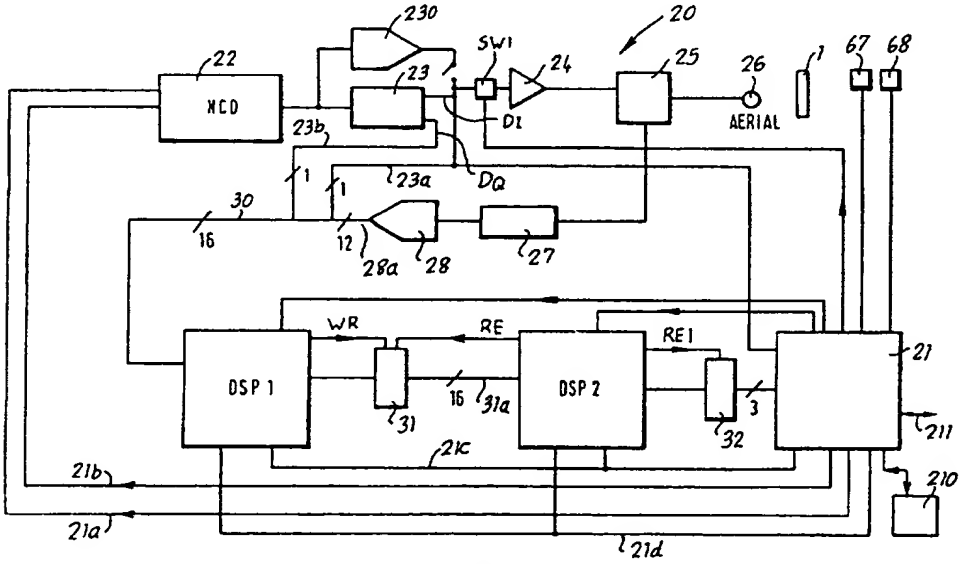

FIG. 6

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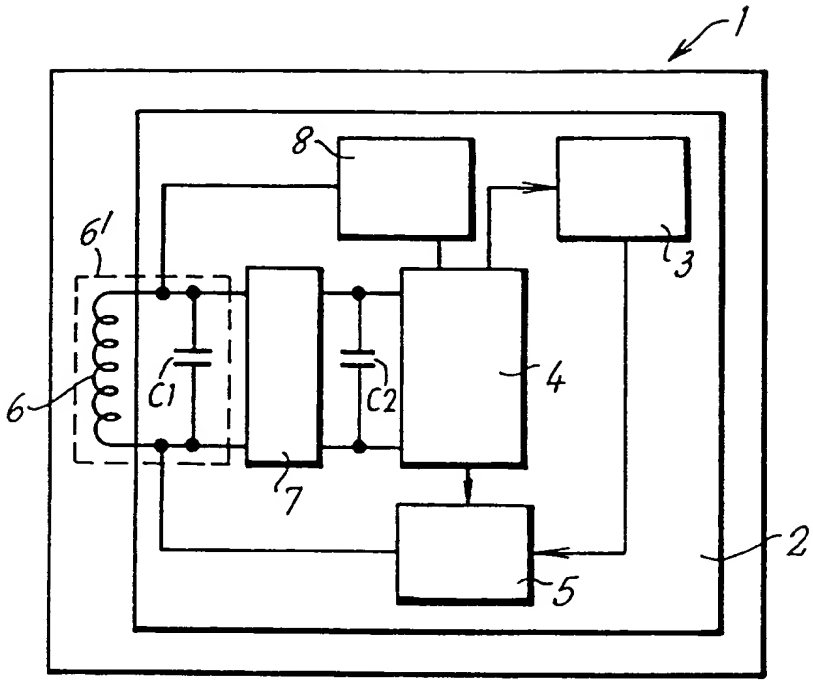


FIG. 1

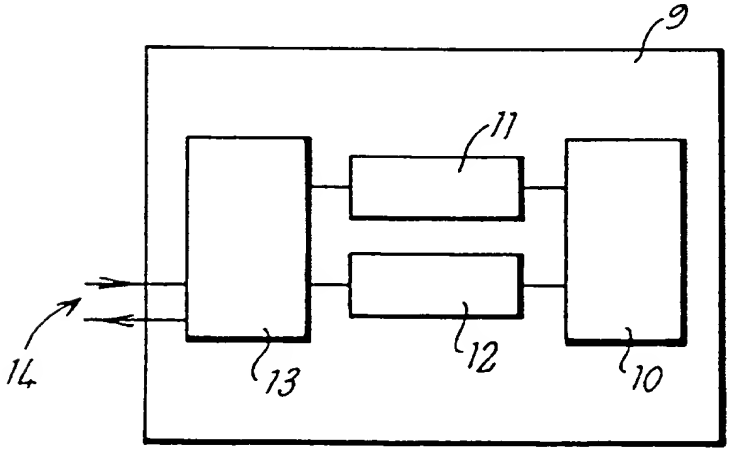


FIG. 2

FIG. 3a

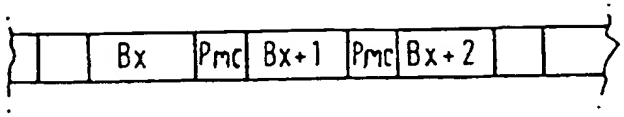
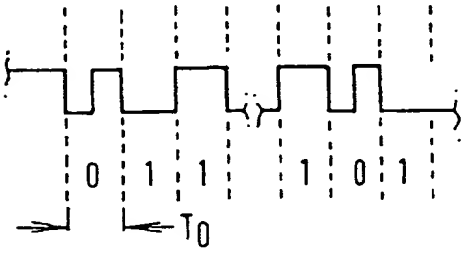


FIG. 3b



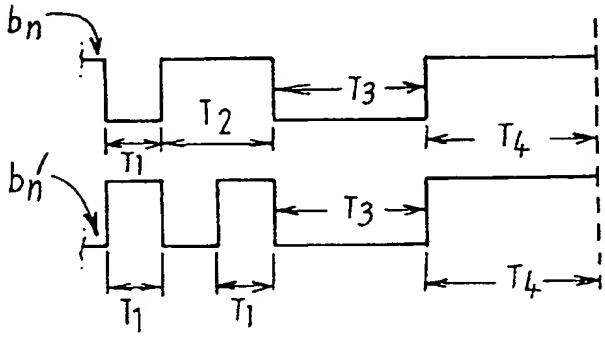


FIG. 3c

FIG. 3d

FIG. 4

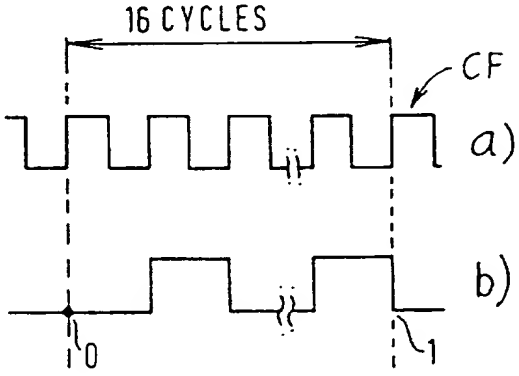
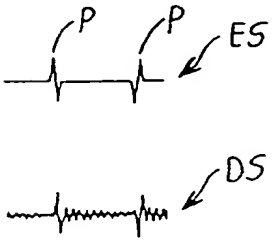


FIG. 5



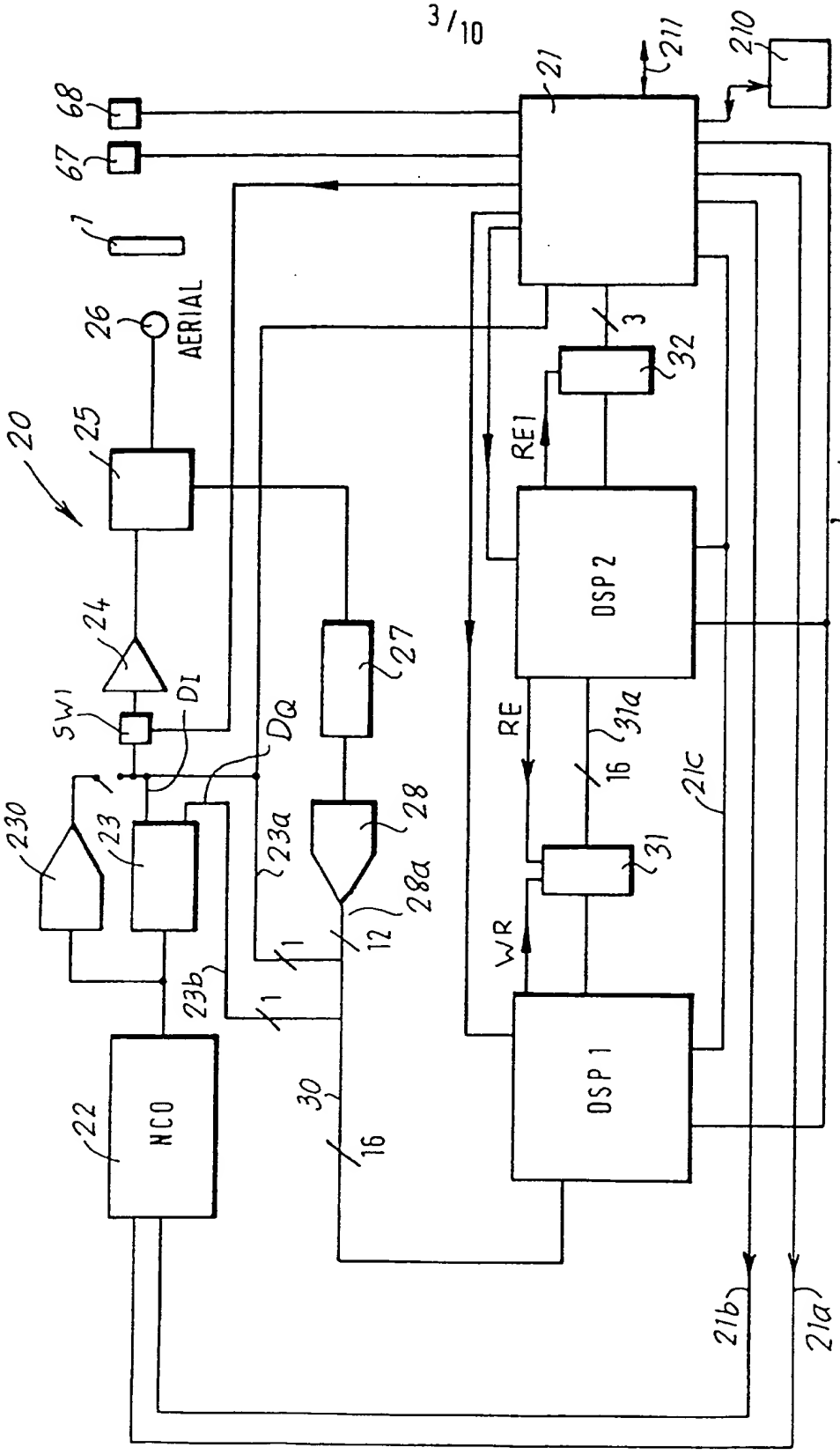

68
67
1
AERIAL
26
20
25
24
SW1
DI
DQ
27
230
23
23a
28
28a
23b
22
NCO
30
16
12
1
1
21
211
210
3
32
RE1
21d
DSP 2
RE
31a
16
21c
31
WR
DSP 1
21b
21a

FIG. 6

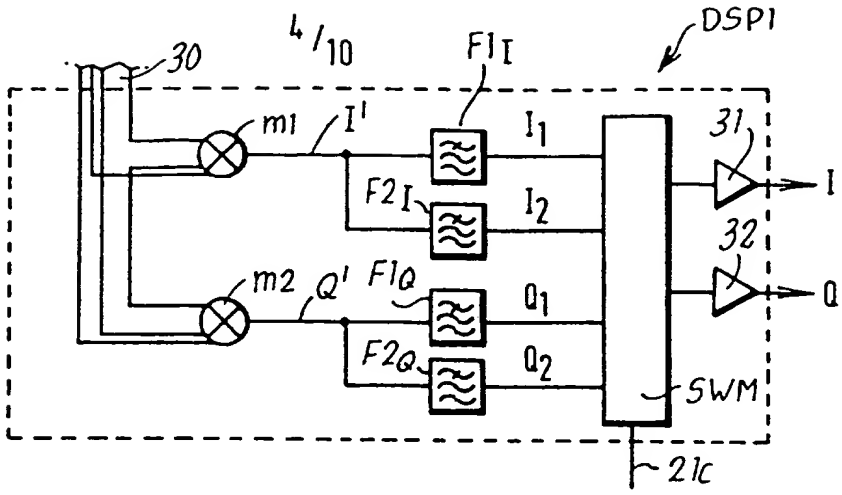


FIG. 7

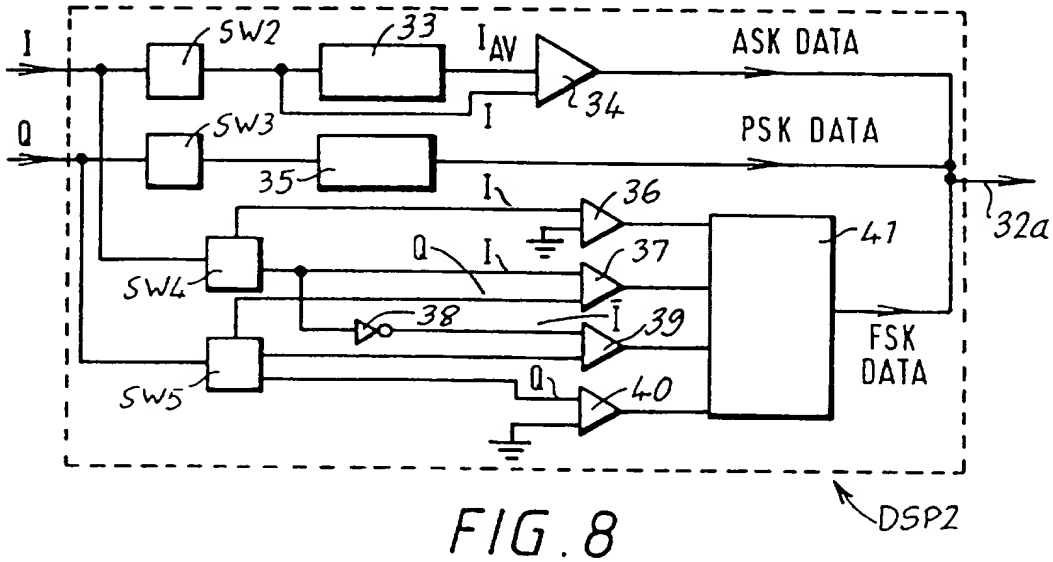


FIG. 8

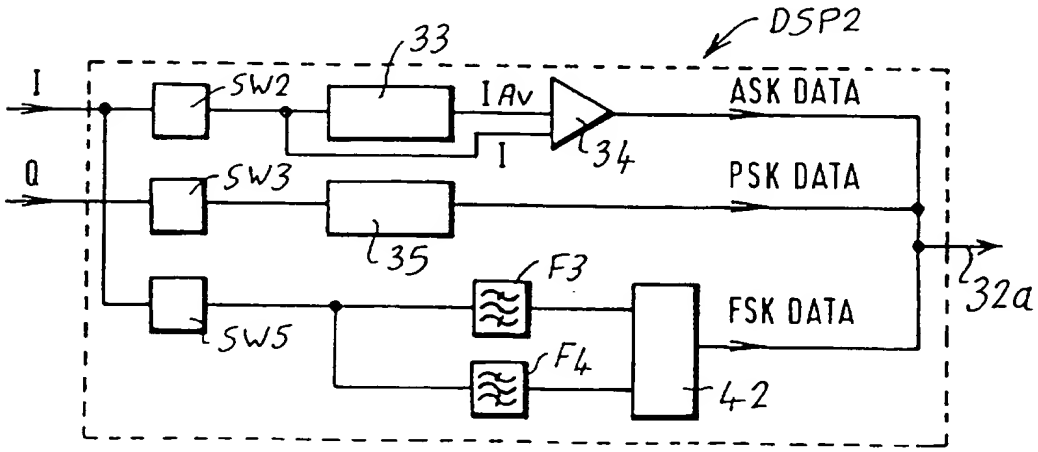


FIG. 9

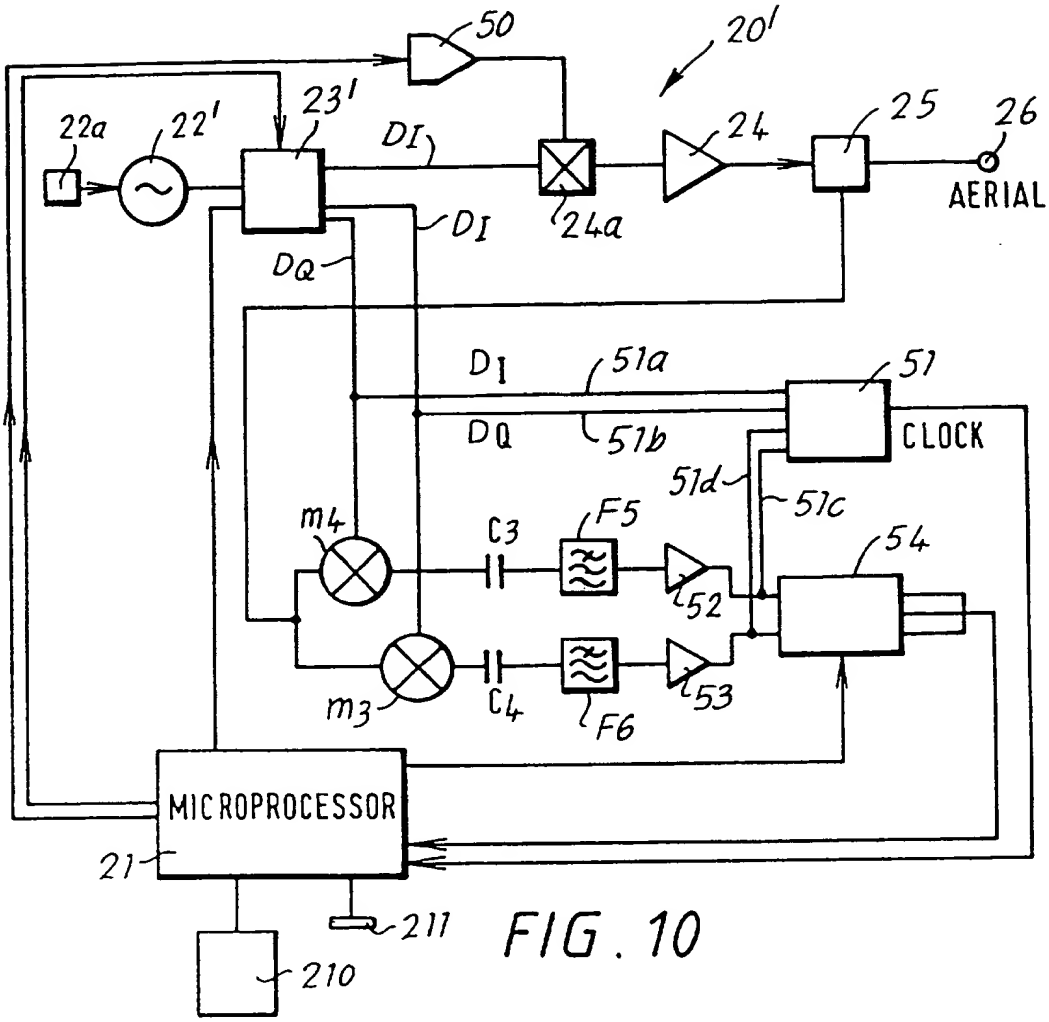

50
20'
22a
22'
23'
DI
24
25
26
AERIAL
24a
DI
DQ
DI
51a
51
DQ
51b
CLOCK
51d
51c
m4
C3
F5
54
52
m3
C4
F6
53
MICROPROCESSOR
21
211
210

FIG. 10

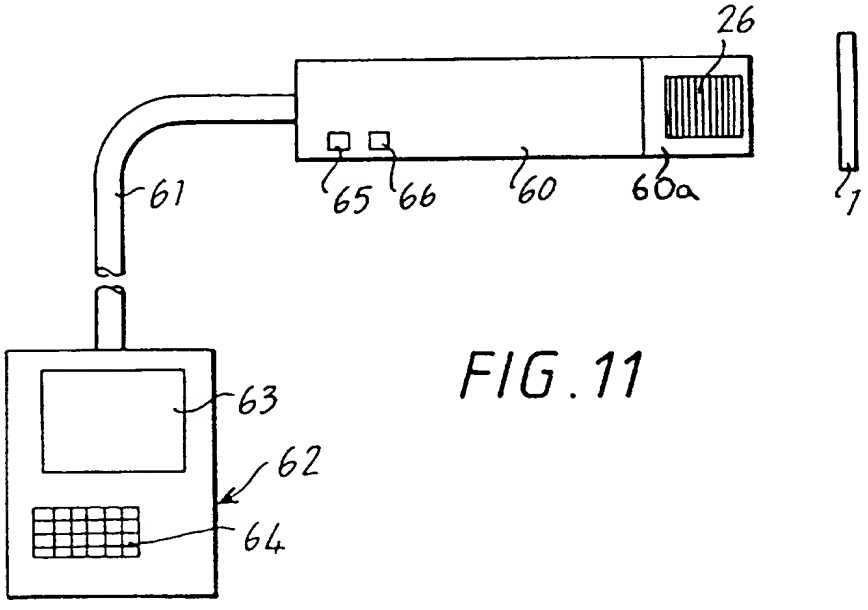

26
61
65
66
60
60a
1
63
62
64

FIG. 11

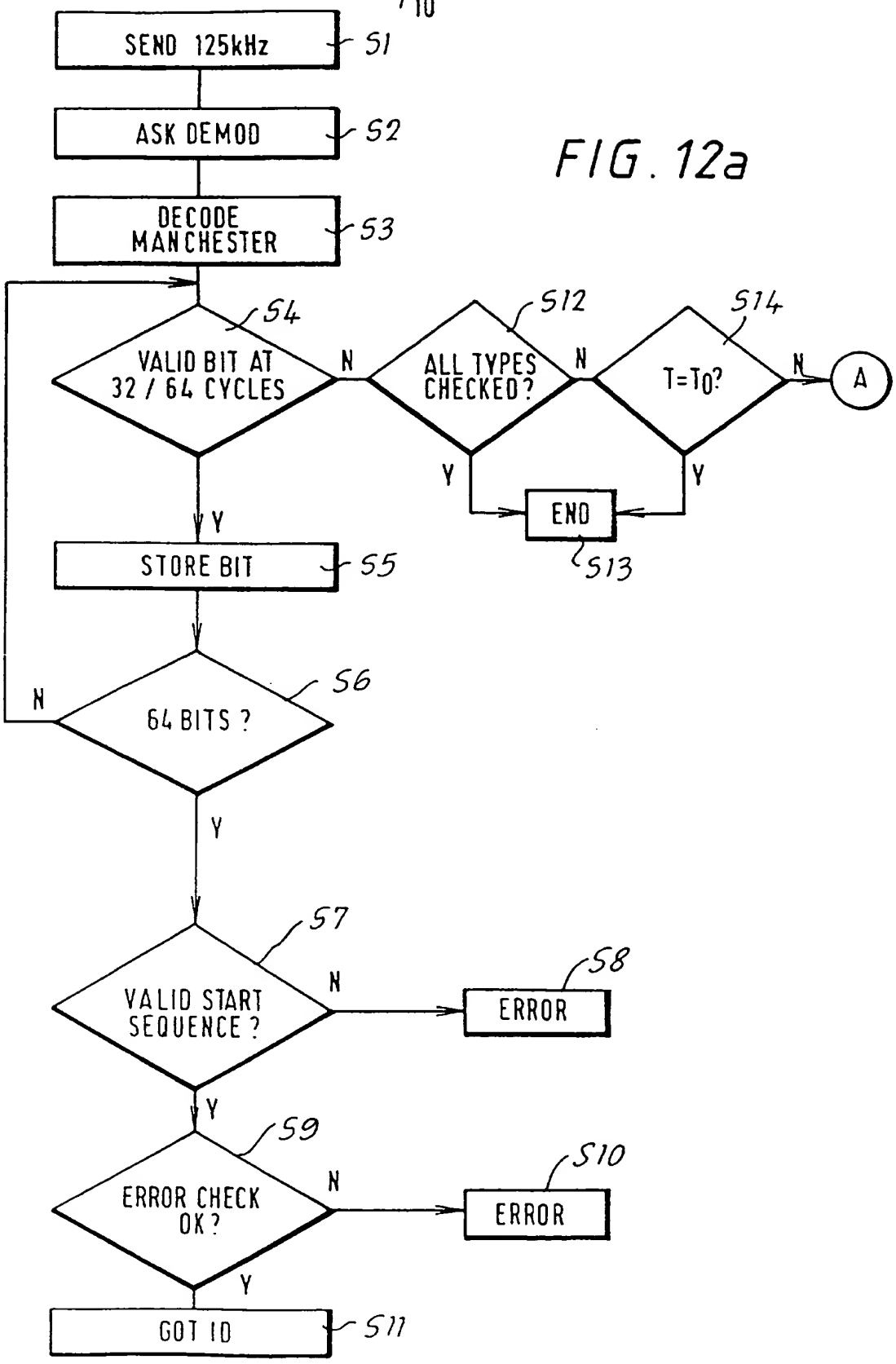

SEND 125kHz
S1
ASK DEMOD
S2
DECODE MANCHESTER
S3
S4
VALID BIT AT 32 / 64 CYCLES
N
S12
ALL TYPES CHECKED?
N
S14
T=T0?
N
A
Y
Y
END
S13
Y
STORE BIT
S5
N
S6
64 BITS ?
Y
S7
VALID START SEQUENCE ?
N
S8
ERROR
Y
S9
ERROR CHECK OK?
N
S10
ERROR
Y
GOT ID
S11

FIG. 12a

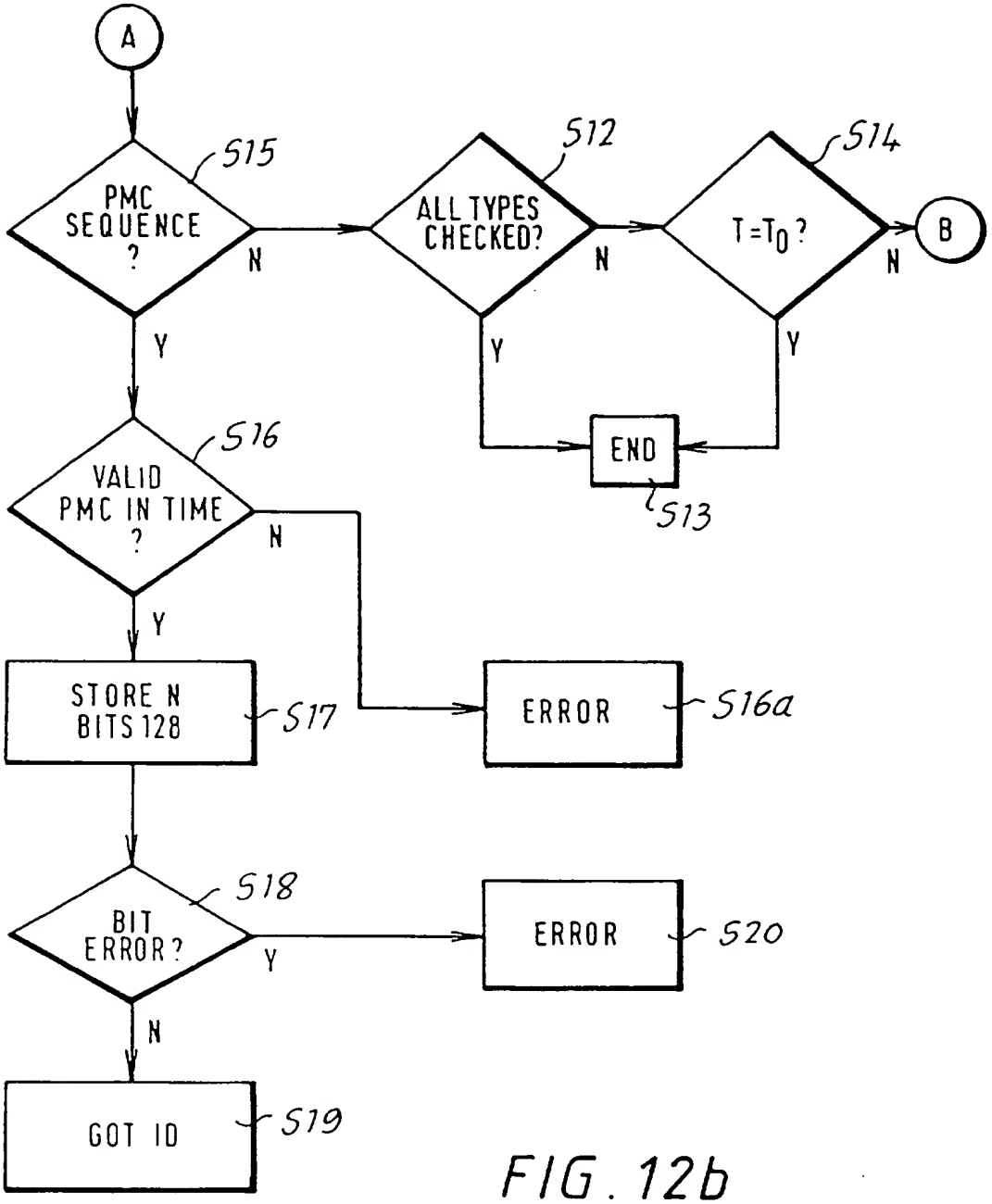

A
S15
PMC SEQUENCE ?
N
S12
ALL TYPES CHECKED?
N
S14
T=T0 ?
N
B
Y
Y
Y
END
S13
S16
VALID PMC IN TIME ?
N
Y
STORE N BITS 128
S17
ERROR
S16a
S18
BIT ERROR?
Y
ERROR
S20
N
GOT ID
S19

FIG. 12b

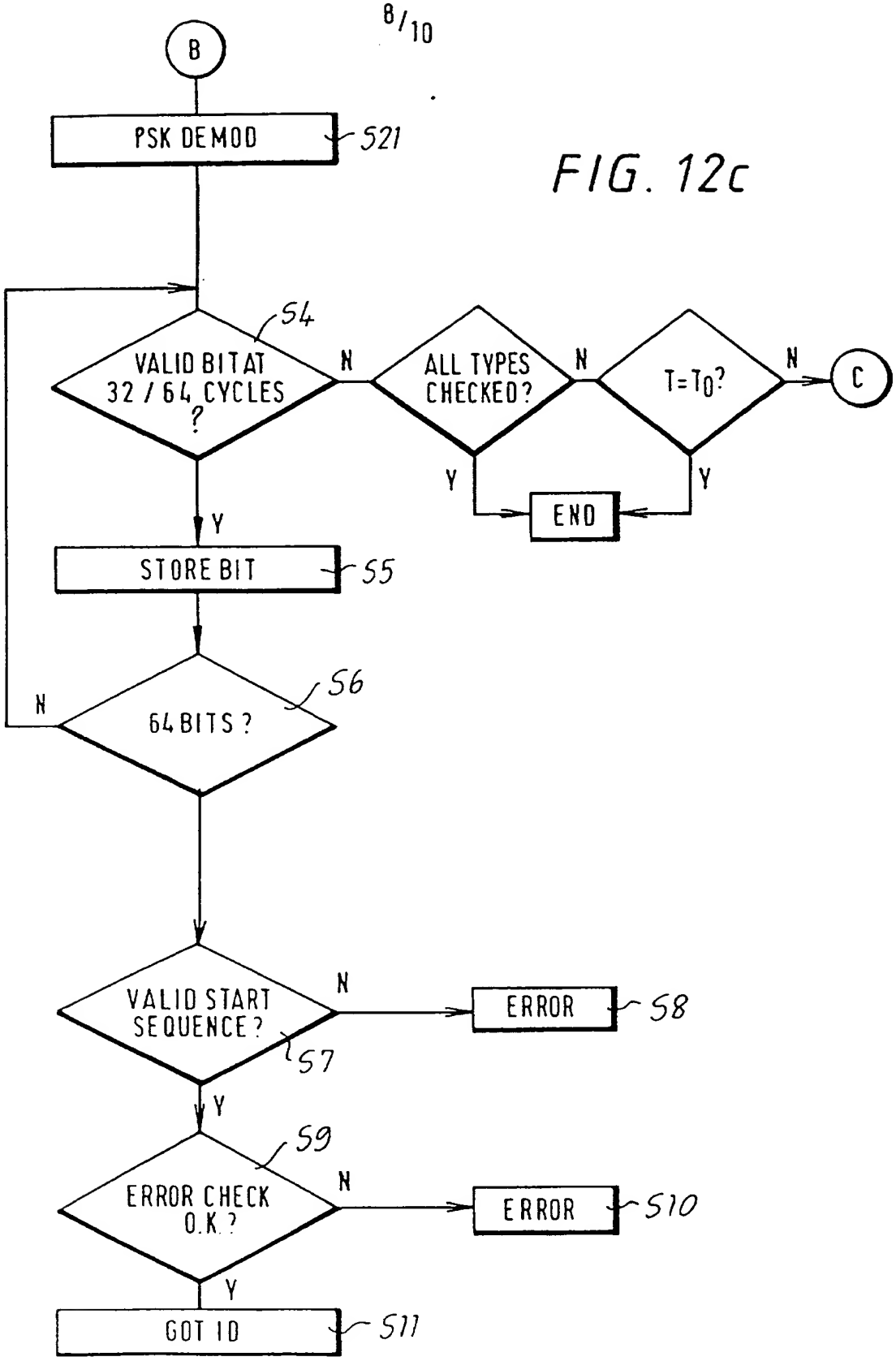
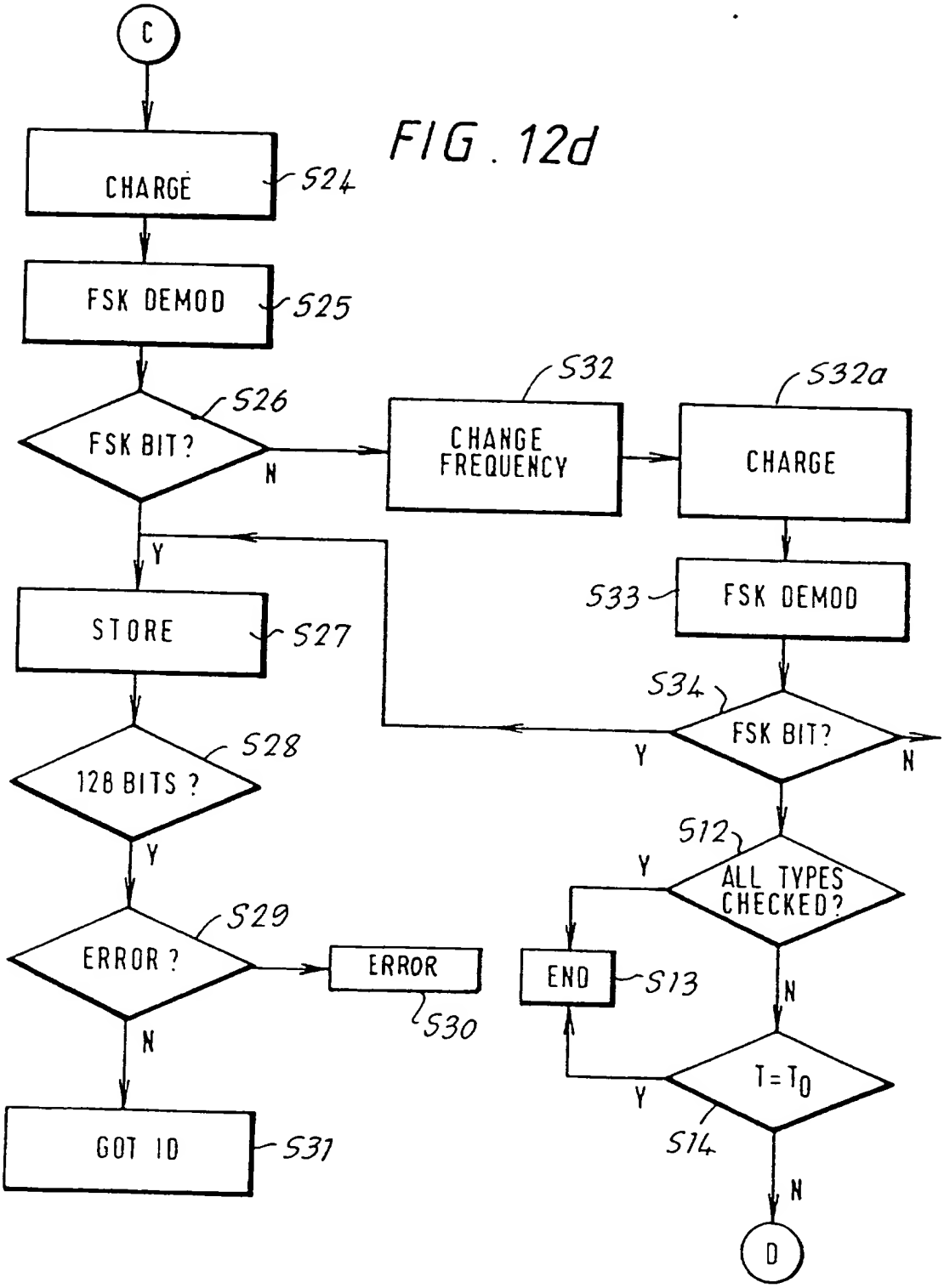

B
PSK DEMOD
S21
S4
VALID BIT AT 32 / 64 CYCLES ?
N
ALL TYPES CHECKED?
N
T=T0?
N
C
Y
Y
END
Y
STORE BIT
S5
S6
N
64 BITS ?
VALID START SEQUENCE?
N
ERROR
S8
S7
Y
S9
ERROR CHECK O.K.?
N
ERROR
S10
Y
GOT ID
S11

FIG. 12c

FIG. 12d


C
CHARGE
S24
FSK DEMOD
S25
FSK BIT?
S26
N
S32
CHANGE FREQUENCY
S32a
CHARGE
Y
STORE
S27
S33
FSK DEMOD
S34
FSK BIT?
Y
N
128 BITS ?
S28
Y
S12
ALL TYPES CHECKED?
Y
N
ERROR ?
S29
ERROR
S30
END
S13
N
T=T0
Y
S14
GOT ID
S31
N
D

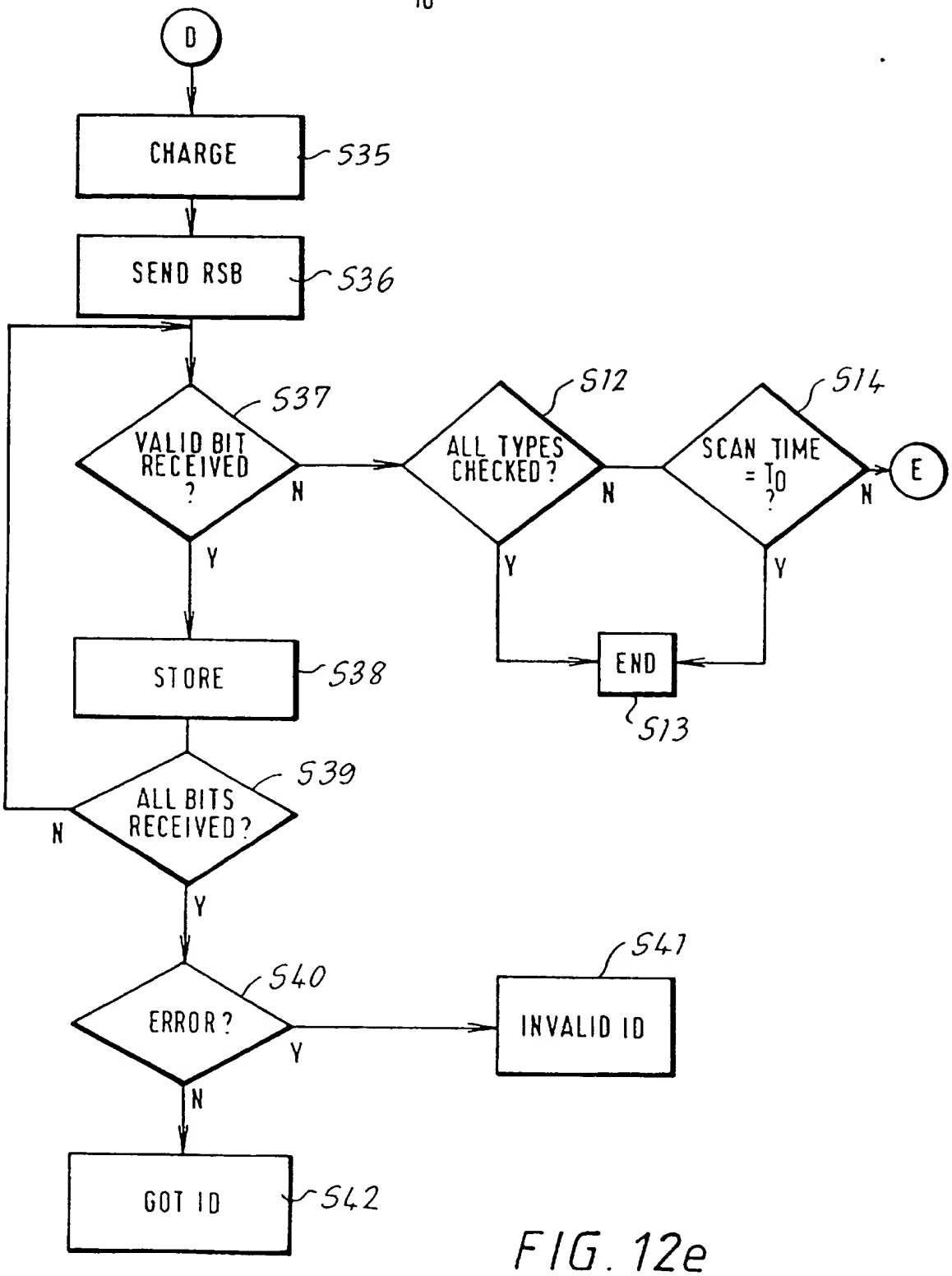

D
CHARGE
S35
SEND RSB
S36
S37
VALID BIT RECEIVED ?
N
Y
S12
ALL TYPES CHECKED ?
N
Y
S14
SCAN TIME = T0 ?
N
Y
E
STORE
S38
END
S13
S39
ALL BITS RECEIVED?
N
Y
S40
ERROR ?
Y
N
S41
INVALID ID
GOT ID
S42

FIG. 12e

APPARATUS AND METHOD FOR REMOTELY READING DATA STORAGE DEVICES

This invention relates to an apparatus and method for remotely reading data storage devices.

Remotely readable data storage devices are particularly attractive for use in enabling identification and tracking of items to which the data storage devices are attached, either permanently or temporarily. One recently developed system for enabling remote reading or interrogation of a data storage device is a radio frequency identification (RF/ID) system in which the data storage device is in the form of a low (LF) or high (HF) frequency tag or transponder with which a reader or interrogator communicates via low frequency radio signals. These tags are passive devices (that is they have no internal power source) and rely on the interrogator or reader to supply the necessary energy to enable operation of the tag.

Figure 1 of the accompanying drawings illustrates a schematic block diagram of a typical example of a tag or transponder 1. The transponder 1 comprises an integrated circuit 2 which is generally formed of silicon. The integrated circuit 2 comprises a non-volatile memory 3, generally a read only memory (ROM) or a non-volatile random access memory (RAM) or FRAM (ferro-electric RAM), for storing data. The memory 3 is

connected to a sequencer or logic control unit 4 which controls the reading or writing of data from the memory 3 and also controls operation of a radio frequency modulation unit 5 for modulating the data for transmission via an RF transmitter in the form of a coil 6 coupled to the integrated circuit 2. The coil 6 also forms the receiver of the transponder 1 and is generally connected to a capacitor C1 to form a parallel resonant circuit tuned to a transmission frequency of a reader compatible with the tag or transponder 1. The output of the resonant circuit 6 is coupled to a rectifier 7 which provides a rectified output for charging a charge storage capacitor C2. The charge storage capacitor C2 is coupled between the positive and negative power supply lines of the integrated circuit. The capacitors C1 and C2 may be integrated in or on the integrated circuit 2 or may be separate components. The RF coil 6 is also coupled to a clock extraction circuit 8 which extracts from an RF signal transmitted to the RF coil a clock control signal for the logic control unit 4. The transponder 1 is provided within an insulating, generally plastics or glass, encapsulation. Typically, the transponder 1 has dimensions ranging from several centimetres down to a few millimetres and may even be as small as, for example, a grain of rice. Such a transponder 1 may easily be incorporated into the packaging or outer casing of products which require identification for stocktaking or

security purposes.

Figure 2 is a block diagram illustrating very schematically the main functional components of a reader or interrogator 9 for reading data stored in the transponder 1. The reader 9 comprises an RF antenna 10 coupled via an RF modulator 11 and a demodulator 12 to a microprocessor control unit 13 which itself may be coupled via an appropriate interface 14 (for example an RS232 interface) to a host computer (not shown). In order to enable data to be read from the tag or transponder 1, the tag or transponder 1 should be placed within a given distance of the antenna 10 of the reader 9 with its RF coil or receiver 6 in an appropriate orientation. The distance depends upon the precise characteristics of the transponder, the strength of the transmitted RF signal and the environment in which it is placed. Typically, this distance may range from about 1-2mm (millimetres) to 1-2 metres. The reader 9 transmits an RF signal of the appropriate frequency which induces an alternating current in the resonant circuit 6' (which as shown by the dashed box consists of the RF coil 6 and the capacitor C1) of the transponder 1 causing the charge storage capacitor C2 to be charged via the rectifier 7. Charging of the charge storage capacitor C2 causes the logic control unit 4 to reset itself and to initiate transmission of an RF signal carrying the data stored in the memory 3 via the modulating circuit

5 and the RF coil 6 for reception by the reader antenna 10.

Currently, there is no common carrier modulation and data transmission system agreed between manufacturers for such transponders and the systems chosen by different manufacturers of tags and readers vary widely and are generally incompatible with one another. This incompatibility means that a reader made by one manufacturer for reading a particular type of tag or transponder will not normally be able to read tags or transponders manufactured by another supplier. This incompatibility is hindering the widespread adoption of the technology because, currently, it is necessary for a customer who wishes to incorporate the tags or transponders into his products to rely on a single source for the transponders and readers. Thus, if the customer's requirements subsequently change or there are commercial reasons for changing to transponders or tags available from different sources, then a severe cost penalty will be incurred in duplicating the reader hardware and software support. In addition, there are many applications for such transponders or tags where it may not be possible to predict in advance the type of tag which will be required to be read by the reader. Such applications include, for example, the identification of lost or stolen property by the police or the tracking or identification of luggage or goods in transit, for

example at airports or across borders.

According to one aspect of the present invention, there is provided apparatus for remotely reading data from a number of data storage devices such as radio frequency identification transponders, which apparatus comprises means for determining the modulation system and/or data transmission system of a data storage device thereby allowing data stored by the data storage device to be read by the apparatus.

In another aspect, the present invention provides a method of remotely reading data from a number of data storage devices such as radio frequency identification transponders which determines the modulation system and/or data transmission system of a data storage device thereby allowing data stored by different manufacturer's data storage devices to be read.

As used herein the term "data transmission system" refers to, for example, the format of the data transmission by the data storage device, that is whether, for example, the data is divided into blocks of data, the relationship between the data and the carrier frequency, the actual carrier frequency and any modulation frequencies where a frequency modulation system is used, whether the data includes headers, parity check bits, block separators and so on and possibly also to any encoding of the data.

Means may be provided for identifying whether the

response signal uses any one of a number of different types of carrier modulation systems by, for example, processing the response signal as if it were using a given one of the different modulation systems and then deciding from the processed signal whether that modulation system was in fact used. If not, the process may be repeated. The decision as to whether a particular modulation system was used may be based on whether or not the processed signal represents a binary data stream of one of the possible carrier modulation and data transmission systems, possibly after suitable decoding. Specific features of the possible data transmission systems may be looked for to enable identification of the actual data transmission system of the data storage device. If no response signal has been received, a signal may be transmitted by the apparatus to the data storage device for a predetermined period to charge the data storage device to see if the data storage device is of a type which requires full charging before it can be read. Also, the frequency of the transmission means may be changed if no response is received at the end of the predetermined period and a determination then made as to whether there is a response from the data storage device to the new frequency. In order to check for data storage devices which require a separate exciter signal after charging, periodic exciter signal bursts may be generated if there is no response after the charging period and a

determination then made as to whether a response signal is received in response to an exciter signal burst.

The apparatus may be housed within a hand-holdable casing. A communications interface may be provided for communication with a host computer. A bar code reader may be incorporated in the apparatus.

Embodiments of apparatus and a method in accordance with the present invention enable a number of different data storage devices, each using a different modulation and/or data transmission system, to be interrogated and read using the response signal transmitted by the data storage device in response to an interrogation signal from the apparatus to identify the modulation and data transmission system of the data storage device and thus enable retrieval of the data transmitted by the data storage device.

Embodiments of the present invention will now be described, by way of example, with reference to the accompanying drawings, in which:

Figure 1 is a block schematic diagram of a typical radio frequency identification tag or transponder;

Figure 2 is a block schematic diagram of a typical radio frequency identification tag reader;

Figure 3a is a block schematic diagram for illustrating the data format for one particular modulation and data transmission system and Figures 3b to 3d are wave form diagrams for that particular

modulation and data transmission system for enabling transmission of data from one type of radio frequency identification tag;

Figure 4 illustrates wave form diagrams for another modulation and data transmission system for transmitting data from another type of radio frequency identification tag or transponder;

Figure 5 illustrates wave form diagrams of another modulation and data transmission system for transmitting data from another type of radio frequency identification transponder;

Figure 6 shows a block schematic diagram of one example of apparatus in accordance with the invention;

Figure 7 shows a functional block diagram for illustrating the operation of a first digital signal processor of the apparatus shown in Figure 6;

Figure 8 shows a functional block diagram for illustrating the operation of one example of a second digital signal processor of the apparatus shown in Figure 6;

Figure 9 shows a functional block diagram for illustrating the operation of another example of the second digital signal processor of the apparatus shown in Figure 6;

Figure 10 shows a block diagram of another example of apparatus in accordance with the invention;

Figure 11 is a diagrammatic view of one possible

form of apparatus in accordance with the invention;

Figures 12a to 12e are flow charts for explaining the operation of an embodiment of apparatus in accordance with the invention.

It should, of course, be understood that the drawings are only schematic and are not to scale. Like reference numerals are used throughout to refer to like components.

Referring now to the drawings, Figures 3a to 3d illustrate schematically components of the modulation and coding scheme used by Philips Semiconductors (a division of Philips Electronics NV of the Netherlands) in its PIT family of radio frequency identification tags or transponders. In the carrier modulation and data transmission system shown in Figures 3a to 3d, the radio frequency identification tag or transponder is responsive to a radio frequency signal at 125kHz and transmits a response signal at the same frequency using amplitude shift key (ASK) modulation. The data is encoded by a diphase coding technique as illustrated schematically in Figure 3b where the interval T_0 represents 16 cycles of the 125kHz carrier signal. As shown in Figure 3b, a binary zero is represented by a change of phase half way through the interval T_0 while a binary 1 is represented by no change of phase within the interval T_0. The data is transmitted in blocks B_x, B_{x+1}, B_{x+2} etc. separated by

program mode check (PMC) sections. Each of the PMC sections incorporates a unique PMC code. There are two types of PMC code depending on whether the last bit of the previous block was of high or low amplitude. Figure 3c shows the situation where the last bit b_n of the previous block ended on a high amplitude. In this case, the PMC code is low for a period T_1 representing 16 cycles of the carrier frequency, is then high for a period T_2 representing 32 cycles of the carrier frequency is then low for a period T_3 representing 128 cycles of the carrier frequency and is then high for a period T_4 representing 127 + 16 cycles of the carrier frequency. As shown in Figure 3d, where the last bit b'_n is or terminates on a low amplitude, the PMC code is high for a period T_1, then low for a period T_1, high again for a period T_1, then low for a period T_3 and high again for the period T_4.

The H4000 ASK family of radio frequency identification transponders manufactured by the Swiss company EM Microelectronic Marin SA also uses an ASK modulation system with a carrier frequency of 125kHz. In this case, however, each bit of the data stream is represented by 64 cycles of the carrier frequency and the data is encoded using Manchester coding so that a logical 1 is represented by modulating the amplitude of the 64 cycles representing the bit so that the amplitude is high

for 32 cycles and then low for 32 cycles and a logical zero is represented by modulating the carrier frequency so that the amplitude is low for 32 cycles and then high for 32 cycles.

The H4000 PSK series of transponders manufactured by EM Microelectronic Marin SA also uses 125kHz carrier frequency but uses a phase shift key (PSK) modulation scheme rather than an ASK modulation scheme. Figure 4 shows wave forms illustrating this modulation scheme. In this case, a bit of the data stream is represented by 16 cycles of the carrier frequency CF shown as waveform a in Figure 4. A 180° change in phase at the end of the 16 cycle period represents, as shown, at b in Figure 4, a logical zero while no change in phase at the end of the 16 cycles represents a logical 1.

In the EM Microelectronic Marin SA modulation and coding systems, the data is represented as 64 bits with a 9 bit header consisting only of logical ones and 40 bits of data arranged as ten columns and four rows with ten row parity check bits, four column parity check bits and one stop bit.

AEG of Germany also produce two families of radio frequency identification (RF/ID) transponders, using 180° PSK and ASK modulation respectively, with the ASK version adopting a Manchester coding system. AEG use a similar scheme data coding to the above-described EM Microelectronic Marin SA system.

Texas Instruments of the United States use a different modulation and coding system which operates on a frequency shift key (FSK) modulation scheme. In this case, the transponder responds to the reader or interrogator only when the transponder detects that its charge storage capacitor has been fully charged. Typically, this takes from 15 to 50 milliseconds. Once the charge storage capacitor has been charged, the transponder transmits its data using a frequency of typically 123.2kHz to represent a logical zero and typically 134.4kHz to represent a logical 1. Each bit is represented by 16 cycles and the identification code carried by the transponder is a 64 bit identification (ID) plus an error check code.

Another transponder which uses an FSK modulation system is manufactured by the Finnish company IDESCO. The data communication system used by this transponder differs from those discussed above in that the transponder must first be charged and then requires a separate exciter signal to be supplied by the reader or interrogator before it will transmit its data. Figure 5a shows the exciter signal ES which consists of a, generally, eight microsecond pulse P which is repeated every 50 microseconds with a 180° phase change in the carrier signal every other pulse. The 180° phase change in the pulse instructs the transponder to send the part of the data bit. Each data bit is thus represented by

a signal supplied by the transponder in response to each of two successive exciter pulses. A logical 1 is represented by a high frequency (300kHz) response to one exciter pulse followed by a low frequency (250kHz) response to the next exciter pulse while a logical zero is represented by a low frequency response to one exciter pulse followed by a high frequency response to the next exciter pulse. The data may be provided as a 64 or 256 bit stream. Figure 5b illustrates part of a data signal DS. The same number of cycles of the high and the low frequency modulation is provided.

Figure 6 illustrates one example of apparatus 20 in accordance with the present invention which is capable of reading at least the transponders described above with reference to Figures 3 to 5.

As shown in Figure 6 the apparatus 20 comprises a microprocessor or microcontroller 21 with associated memory 210 (for example ROM and/or RAM) which controls the overall operation of the apparatus and stores information relating to the carrier modulation and data transmission systems of the various tags or transponders which the apparatus is designed to read.

The apparatus 20 comprises a numerically controlled oscillator (NCO) 22 which, under the control of the microprocessor 21, outputs a digital signal which has a frequency four times that of the desired carrier frequency. The output of the NCO 22 is supplied to a

programmable logic device or scaler 23 which has first and second outputs D_I and D_Q. The first output D_I is a binary digital signal which changes state (i.e. changes between 0 and 1) at the leading (or trailing) edge of every fourth pulse from the NCO 22 to provide a digital binary signal of the required carrier frequency. The second output D_Q of the scaler 23 similarly changes state at the same frequency. However, the change of state of the output D_Q is 90° out of phase with the output D_I, that is the second output D_Q changes phase on the leading (or trailing) edges of the first, fifth, ninth, etc. output pulses from the NCO 22. The outputs D_I and D_Q are supplied by respective one bit data buses 23a and 23b to a 16 bit data bus 30. The data bus 23a is also coupled to the microprocessor to provide to the microprocessor a signal representing the clock frequency of the tag or transponder. The output D_I of the scaler 23 is also supplied via a switch SW1 to a power amplifier 24 which is coupled via an RF directional coupler 25 to an RF antenna 26.

The antenna 26 may comprise a single RF coil with an inductance of, typically, 186 milli Henrys. Although not shown, as another possibility, the antenna 26 may consist of a number of RF coils (which may be provided by connecting tap points to a single coil) with the particular coil or combination of coils being selected

by switches controlled by the microprocessor 21. This enables the RF coil characteristics to be optimised for transmission of signals to and reception of signals from different transponders or tags 1.

The power amplifier 24 and RF antenna 26 provide a resonant circuit for generating an RF sinusoidal signal from the binary digital signal supplied via the scaler 23. As an alternative to using the scaler 23 to provide the RF signal for transmission by the transmitter 26, a digital to RF converter 230 may be coupled between the NCO 22 and the switch SW1 to convert the digital output signal from the NCO 22 into an RF sinusoidal signal of a quarter the frequency.

As indicated above, the actual frequency supplied by the NCO 22 is controlled by the microprocessor 21 via data and clock lines 21a and 21b. The microprocessor 21 may also enable switching on or off of the NCO for power saving reasons.

The RF directional coupler 25 prevents, as is known in the art, an RF signal received by the antenna 26 from being supplied back to the power amplifier 24. This enables the same antenna 26 to be used for both transmission and reception of RF signals. Of course, if desired, separate transmission and reception aerials could be provided.

An RF signal received via the antenna 26 is supplied via the directional coupler 25 to an analog-to-digital

converter (ADC) 28 via a conditioning circuit 27 which comprises conventional filters for removing noise components from the received RF signals. The analog-to-digital converter (ADC) 28 has a 12 bit parallel output data bus 28a which is coupled to the 16 bit parallel data bus 30 with the one bit data buses 23a and 23b. The data bus 30 is coupled to the input of a first digital signal processing unit DSP1. As will be explained below, the first DSP1 serves to mix or multiply each of the binary digital output signals D_I and D_Q with the data carrying digital output signal of the ADC 28 to provide an in-phase data carrying signal I and a quadrature out-of-phase data carrying signal Q. The data carrying digital signals I and Q are supplied one after another to a first latch or FIFO buffer 31 which is coupled via a 16 parallel bit data bus 31a to a second digital signal processor DSP2 which, as will be explained below, affects appropriate demodulation processing of the I and Q data carrier signals to enable data extraction. The output of DSP2 is coupled via a second latch 32 to the microprocessor 21. Typically, the DSPs may be TMS 320C 52 or possibly TMS 320C 25 DSPs produced by Texas Instruments.

Figure 7 is a functional block diagram for explaining the operation of the DSP1.

As shown in Figure 7, the 16 bit parallel data bus 30 is divided upon input into the DSP1 so that the 12 bit

data carrying digital signal from the DAC 28 is mixed by the in-phase binary digital signal D_I and the quadrature out-of-phase binary digital signal D_Q, respectively. This process is illustrated by mixers M1 and M2 in Figure 7. The mixing process represented by the mixer M1 provides an in-phase data carrying signal I' while the mixing process illustrated by the mixer M2 provides a quadrature out-of-phase data carrying signal Q'. The data carrying signals I' and Q' are then low-pass filtered by finite impulse response filter functions of the DSP1 which are designed to remove the carrier frequency and would, in the absence of any data signal, output a signal of constant amplitude representing the amplitude of the carrier frequency. Although the filter functions applied to each of the signals I' and Q' will be the same, the particular filter required to remove the carrier frequency may depend upon the particular type of transponder being read. For this reason, Figure 7 shows each of the signals I' and Q' as being coupled to the input of two low-pass filters $F1_I$ and $F2_I$ for the signal I' and $F1_Q$ and $F2_Q$ for the signal Q'. The filters produce output signals I_1, I_2, Q_1 and Q_2 which are selectable under the control of signals input to the DSP1 via a control line 21c of the microprocessor. This function of the DSP1 is represented by a multiplexing switch SWM in Figure 7 which provides, via amplifiers 31

and 32, an in-phase data carrying signal I and a quadrature out-of-phase data carrying signal Q selected from the signals I_1 and I_2 and Q_1 and Q_2, respectively.

As explained above, the in-phase and quadrature out-of-phase signals I and Q are supplied one after another via the latch 31 to the second DSP2. The latch 31 is provided to control the data flow rate between DSP1 and DSP2 to enable DSP2 to carry out its data processing. If, however, the DSP2 is capable of operating sufficiently quickly, then it may be possible to dispense with the latch 31. The flow of data between DSP1 and DSP2 and the microprocessor 20 may also be controlled by signals from the microprocessor on line 21d.

The DSP2 is programmed to extract the data from the in-phase and quadrature out-of-phase data carrying signals I and Q and to provide the microprocessor, via the latch 32, with a demodulated digital data stream of noughts and ones which the microprocessor can then identify or decode as will be described below with reference to Figure 12.

Figure 8 is a block diagram for illustrating one way in which the DSP2 may be programmed so as to obtain the raw binary data (which may or may not be coded) from the in-phase and quadrature out-of-phase data carrying signals I and Q which may be ASK, PSK or FSK modulated. The DSP2 carries out different data extraction routines depending upon whether the incoming data carrying signals

are assumed to be ASK, PSK or FSK modulated. Selection of the data extraction routine of the DSP2 is under microprocessor control via the control line 21c and this is illustrated functionally in Figure 8 by means of microprocessor-controlled switches SW2 to SW5 which control supply of the input data carrying signals I and Q to the various data extraction routines of the DSP2.

In order to extract the raw binary data from an ASK modulated data carrying signal, the DSP2 performs a running average (over, for example, 50 milliseconds) of the in-phase data carrying signal I (as illustrated functionally in Figure 8 by the averaging circuit 33) to provide an average signal I_{AV}. The DSP2 then compares this average signal I_{AV} with each bit of the input in-phase data carrying signal I as represented by the comparator 34 in Figure 8 and provides an output signal which is 1 when the bit of the input data carrying signal I is greater than the average I_{AV} and is zero when the bit of the input data carrying signal I is smaller than the average I_{AV}. The average I_{AV} is constantly updated by the DSP2 and a hysteresis circuit is included so as to avoid hunting or cycling. ASK demodulated data is output on output line 32a to the latch or FIFO buffer 32 for supply to the microprocessor. As another possibility, the DSP2 may also perform the averaging and comparison steps on the quadrature out-of-phase data carrying signal

Q to provide the ASK demodulated binary data. This may be done additionally or in place of the processing of the in-phase data carrying signal I. If the averaging and subsequent comparison are carried out on both the in-phase and the quadrature out-of-phase data carrying signals I and Q, the DSP2 may then select whichever of the two ASK demodulated binary data streams is less noisy or otherwise provides the stronger signal or may vectorally add them.

Where the modulation used to transmit the data is the 180° PSK system discussed above with reference to Figure 4, then the effect of mixing the output of the ADC 28 with the quadrature out-of-phase digital signal D_Q is to provide a signal which goes positive or negative depending upon whether the PSK modulated carrier undergoes a 180° phase shift or not. The raw binary data can therefore be derived from the quadrature out-of-phase data carrying signal Q simply by appropriate threshold and level detecting as indicated by the circuit 35 in Figure 8 to provide an output which is 0 when the quadrature out-of-phase data carrying signal Q is high and 1 when the quadrature out-of-phase data carrying signal is low. Again, the PSK demodulated binary data is supplied from the DSP2 to the latch 32 on output line 32a. The in-phase data carrying signal I could also be used to extract PSK modulated data but is less sensitive

because the signal changes only between zero and a positive value in accordance with the PSK modulated data.

Figure 8 illustrates by functional components one possible data extraction routine which may be used by the DSP2 to demodulate FSK modulated data. As discussed above, in the FSK modulated data, zeros and ones are represented by different frequency modulations of the carrier signals. Where the carrier signal frequency is intermediate to modulation frequencies or, as will be described below, the frequency supplied by the scaler 23 for mixing with the output of the ADC 28 is adjusted so as to be between the two modulation frequencies, then the fact that the phase difference between the carrier frequency and the higher modulation frequency will change in one direction with time whereas the phase difference between the carrier frequency and the lower frequency modulation signal will change in the other direction with time means that the modulation frequency can be detected by determining the direction of phase change in the I and Q data carrier signals. Thus, by comparing, as indicated functionally in Figure 8 by the comparators 36 and 40, the amplitudes of the in-phase and quadrature data carrying signals I and Q with zero (indicated by the earth or ground symbols in Figure 8) output signals can be obtained which increase or decrease with time depending upon the direction in which the phase is changing. To increase the accuracy of this approach, the

in-phase data carrying signal may be compared with the quadrature data carrying signal as illustrated by the comparator 37 in Figure 8 and the inverted (as indicated functionally in Figure 8 by the inverter 38) in-phase data carrying signal $\bar{I}$ may be compared with the quadrature out-of-phase data carrying signal Q as indicated by the comparator 39. The results of these comparisons are used by the DSP2 to determine whether the phase is increasing or decreasing with time and so to determine whether the modulation frequency is higher or lower than the carrier frequency. DSP2 outputs a logical 1 when the modulation frequency is higher than the carrier frequency and a logical zero when the modulation frequency is lower than the carrier frequency. This function is illustrated in Figure 8 by logic circuitry 41.

Figure 9 illustrates a functional block diagram for illustrating different possible data extraction processes for the DSP2. The functional block diagram shown in Figure 9 differs from that shown in Figure 8 only in respect of the data processing routine used to extract the FSK binary data. In the example shown in Figure 8, when the microprocessor 21 instructs the DSP2 to carry out FSK modulated data extraction, the in-phase data carrying signal I is supplied to two band pass filters F3 and F4 which may be implemented using Goetzel's algorithm in the DSP2. The filters F3 and F4 each pass

one of the two modulation frequencies. The DSP2 outputs, as indicated by logic circuitry 42 in Figure 9, a logical zero when there is an output from one of the filters F3 and F2 and a logical 1 when there is an output from the other of the filters F3 and F4. Although this approach may be simpler in terms of processing complexity than the arrangements shown in Figure 8, it does require that the filters F3 and F4 have narrow well-defined band pass regions.

In the example described above with reference to Figures 6 to 7, the apparatus is implemented as a digital circuit. It is, however, possible to implement at least some of the components of the apparatus as analog circuits. Figure 10 is a block diagram illustrating apparatus embodying the invention which is implemented at least in part by analog circuits.

As shown in Figure 10, in this example the apparatus 20' comprises a conventional voltage controlled tunable oscillator 22' in which the operating frequency is controlled by voltage variable capacitors (varactors) with the voltages applied to the varactors from a controllable voltage source 22a being controlled by the microprocessor 21. The output of the oscillator 22' is applied to a digital signal processor 23' which performs similar functions to the scaler 23 in the apparatus shown in Figure 6. Thus, the oscillator 22' is controlled to provide a frequency four times that of the desired

carrier frequency and the digital processor 23' provides the in-phase and quadrature out-of-phase digital signals D_I and D_Q at the carrier frequency. The in-phase digital signal D_I is supplied via a variable gain amplifier stage 24a to the power amplifier 24 as in Figure 6. The gain of the variable gain amplifier stage 24a may be controlled by a digital-to-analog converter 50 which is controlled by the microprocessor 21. The variable gain amplifier stage 24a may be used to boost or reduce the power of the carrier frequency signal if the microprocessor determines that a tag or transponder is not responding correctly.

As in the example described with reference to Figure 6, the output of the power amplifier 24 is supplied to the RF antenna 26 via an RF directional coupler 25. When an incoming data carrying RF signal is received by the antenna 26, the directional coupler 25 supplies the data carrying signal to each of first and second mixers M3 and M4. The first mixer M3 also receives the in-phase digital signal D_I while the second mixer M4 also receives the quadrature out-of-phase digital signal D_Q. In this example, the mixers M3 and M4 may be in the form of comparators or differential amplifiers with one of the positive and negative inputs of each comparator receiving the data carrying RF signal from the antenna 26 and the other receiving the appropriate one of the digital

signals D_I and D_Q. The outputs of the mixers M3 and M4 are supplied to respective programmable filters F5 and F6 via decoupling capacitors C3 and C4 which act to remove reader transmit signal leakage appearing as DC at the output of the mixers. Although not described above with reference to Figures 6 to 9, the DSP1 may include functions analogous to the decoupling capacitors C3 and C4. The filters F5 and F6 are arranged to pass the modulated data without the carrier signal. That is, if no data were present on the signal received by the antenna 26, the outputs of the band-pass filters F5 and F6 would have a constant level dependent upon the amplitude of the carrier. Although not shown in Figure 10, as in the example described with reference to Figure 6, each of the filters F5 and F6 may comprise a number of separate individual filters with the actual filters used to filter the outputs of the mixers M3 and M4 being determined in accordance with instructions from the microprocessor 21. The outputs of the filters F5 and F6 are supplied via amplifiers 52 and 53 to a data extraction circuit 54. The data extraction circuit may comprise respective analog-to-digital converters (not shown) for the outputs of the amplifiers 52 and 53 together with a digital signal processor similar to the DSP2 shown in Figures 6 and 8 or 9.

The binary in-phase and quadrature out-of-phase signals D_I and D_Q and the in-phase and quadrature out-of-

phase data carrying signals I and Q may also be supplied on respective lines 51a, 51b, 51c and 51d to a clock extraction circuit 51 which is in the form of a digital signal processor which determines from these signals the clock frequency of the transponder 1. This circuit may, although not shown, also be provided in the apparatus shown in Figure 6. The clock extraction circuit 51 is generally not needed except in the cases of transponders such as the Texas family of TIRIS transponders in which the clock frequency changes with the high and low frequency modulation so as to enable the high and low frequency modulation sections of a bit each to consist of the same number of cycles.

The apparatus 20 shown in Figure 6 or the apparatus 20' shown in Figure 10 would generally be mounted onto a single printed circuit board using surface mounted components where available.

The apparatus may, as shown in Figure 11, be mounted in a compact plastics case 60 which, as shown in Figure 11, is preferably in the form of a tube so that the apparatus can be handled conveniently. Indeed, the apparatus 20 may, as illustrated schematically in Figure 6, be provided with a light emitting device (generally a laser) 67 and a photosensitive device 68 to enable, by incorporation of suitable software into the microprocessor's programming, the apparatus also to be used to read conventional bar codes. The bar code

reading may be carried out simultaneously with the RF tag reading by using time share processing or an interrupt protocol, for example.

The microprocessor or microcontroller is provided with a serial interface 211 generally an RS232 interface. Power supply to the apparatus and connection of serial data to the RS232 interface is by way of a flexible cable 61 coupling the apparatus to a commercially available portable computer for example a laptop or palmtop personal computer or a portable data terminal (that is a small hand held computer which has been made rugged for use in industrial environments) such as a Psion organiser 62 with a liquid crystal or similar display screen 63 and an input or input devices in the form of a keyboard 64 and possibly also a track ball or similar pointing device. Such an arrangement allows the apparatus to be fully portable enabling it to be moved to the location of the tag or transponders to be identified. This should be of particular advantage where, for example, it is necessary to check the tags or transponders carried by a large consignment of goods or to check the tags or transponders of heavy or bulky items which are difficult to move.

Of course, the apparatus may be connected via the RS232 interface to other suitable host computers, for example a desktop personal computer in appropriate circumstances. Also, the apparatus may be built into a

portal or like device through which a conveying belt carrying items to be identified or luggage to be checked passes.

As shown in Figure 11, the antenna 26 of the apparatus is provided at one end of the housing 60 and might be of any suitable conventional design. In addition, the housing 60 carries a green LED 65 and a red LED 66, both of which are actuable by the microprocessor. The green LED is designed to be lit to indicate that power is being supplied to the apparatus 1 while the red LED may be illuminated to indicate that a tag has been read. One or both of the LEDs or a separate LED may be actuated or caused to flash by the microprocessor 21 in the event of a fault condition such as a short or open circuit in the antenna.

The portion 60a of the housing carrying the antenna 26 is detachable and may be replaced by an electrically equivalent antenna of smaller physical dimensions to allow more versatile searching in confined spaces.

In use of the apparatus shown in Figure 11, a tag or transponder 1 to be read and the antenna 26 should be positioned so as to be a maximum distance of 50mm apart where the tag has a nominal diameter of 25mm. The wand is designed so that optimum coupling should occur when, in the case of a disk-like tag, the major surfaces of the tag are parallel to the end of the cylindrical housing 60 as shown in Figure 1. The user may then operate the

keyboard 64 to instruct the microprocessor 21 via the RS232 interface that it is desired to read the data stored in the tag or transponder 1. Alternatively, the microprocessor 21 may be programmed or instructed to search or seek for tags or transponders. This latter option is particularly suitable for use where the tags or transponders are carried by goods conveyed past a station at which the apparatus is located.

The following description relates to the digital implementation of the apparatus shown in Figures 6 to 9. However, it will be appreciated by those skilled in the art that the operation of the apparatus shown in Figure 10 is similar.

Once the microprocessor has been instructed via the RS232 interface that a tag or transponder 1 is to be read or has been instructed to search or seek for tags, the microprocessor 21 sends signals via the control lines 21a and 21b to switch on the numerically controlled oscillator 22 and to cause the numerically controlled oscillator to generate a signal with a frequency of four times 125kHz so that the scaler 23 provides a 125kHz digital signal to the amplifier 24 via the switch SW1. The antenna 26 therefore transmits a sinusoidal RF signal at 125kHz to the tag or transponder 1 as indicated at step S1 in Figure 12a. As indicated above, where the antenna 26 comprises a selectable RF coil arrangement, the microprocessor 21 will also select the RF coil or

coils most suitable for transmitting signals to and receiving signals from the particular tag or transponder 1 which the microprocessor initially assumes is present.

Any return signal transmitted by the tag or transponder 1 is supplied via the antenna 26, directional coupler 25, conditioning circuit 27 and ADC 28 to the DSP1 which is controlled by the microprocessor 21 produce the in-phase and quadrature out-of-phase data carrying signals I and Q from which the 125kHz carrier frequency has been filtered out. The in-phase and quadrature out-of-phase data carrying signals I and Q are written into the latch 31 under the control of write signals supplied via a write line WR from the DSP1. Data is supplied from the latch 31 up to the DSP2 on the 16 parallel bit data bus 31a in response to a read instruction received from the DSP2 along the read line RE. The microprocessor 21 first assumes that the data transmitted by the tag or transponder 1 is ASK modulated and therefore controls the DSP2 to process the incoming in-phase data carrying signal I as ASK modulated data at step S2. The ASK demodulated binary data is supplied via the DSP2 to the latch 32 under control of a read signal RE1 from the DSP2 and thence to the microprocessor 21. The microprocessor initially assumes, in this example, that the tag or transponder being read is produced by EM Microelectronic Marin SA and therefore assumes that the digital data stream supplied by the DSP2 is Manchester code encoded.

The microprocessor thus decodes the received data as if it were Manchester encoded data at step S3 and then checks to see if a valid 0 or 1 data bit at a frequency of 32 or 64 cycles per second has been received at step S4. If the answer is yes, the microprocessor stores the bit in RAM (not shown) at step S5 and then checks to see whether 64 bits of data have been received at step S6. If the answer is no, the microprocessor repeats steps S4, S5 and S6 until 64 bits of data have been received. The microprocessor then looks at step S7 for a valid start sequence in the 64 bits of received data. That is, the microprocessor looks for the characteristic 9 logical 1 bits header of the EM Microelectronic Marin SA data storage format. If a valid start sequence is not detected, the microprocessor indicates at step S8 that an error has occurred and may cause one or both of the LEDs on the wand to flash. In addition, the microprocessor may supply signals via the RS232 interface to cause an error message to be displayed on the LCD 63 of the host computer 62. Assuming a valid start sequence is detected, the microprocessor then checks the parity bits at step S9 in accordance with the stored information regarding this type of tag to determine whether there are any errors in the received data. If the error check is not OK, that is if an error is detected, the microprocessor causes an error message to be generated. Again, for example, one or more of the LEDs 65 and 66 may

be caused to flash and a message may be displayed on the LCD screen 63. Assuming the error check does not indicate any errors in the data, the microprocessor determines that the tag or transponder 1 was indeed of the EM Microelectronic Marin SA ASK modulated family and transmits the decoded data or ID at step S11 to the host computer 62 for display on the screen 63.

If the microprocessor does not detect receipt of a valid bit at step S4, a check is carried out step S12 to determine whether the received data has been analysed on the basis of all types of tag or transponders known to the microprocessor. If the answer is yes, then the microprocessor determines that the tag or transponder 1 cannot be identified and the identification process is terminated at step S13. The microprocessor 21 may also instruct the host computer to display a message indicating that the tag could not be identified. If it is determined at step S12 that the apparatus has not checked for all possible types of tag or transponder known to the apparatus, then the microprocessor first checks at step S14 whether a maximum time T_0 set for the identification process by the user has been exceeded. If the answer is yes, then the microprocessor proceeds to step S13 and indicates that the tag or transponder 1 could not be identified. If the answer at step S14 is no, the microprocessor then checks whether the tag or transponder 1 is another type of tag or transponder 1

using ASK modulation. If desirable, where the antenna 26 has a selectable RF coil arrangement, the microprocessor 21 may modify the RF coil selection to optimise transmission of signals to and reception of signals from the next type of transponder. In particular, in the example shown in Figure 12b, the microprocessor 21 checks the data received from the DSP2 to determine whether it can identify the PMC sequence unique to the Philips PIT family of transponders. If the answer is yes at step S15 and it is determined that a valid PMC was received in the requisite time at step S16, then the microprocessor stores the 128 bits of a block of the PIT data format at step S17 and checks at step S18 to determine whether there is any bit error in accordance with the information stored in its memory concerning this particular type of tag. If the answer is no, the microprocessor 21 determines that the tag has been identified at step S19 and proceeds to decode the data from the DSP2 assuming that the tag is a Philips PIT family tag and supplies the decoded data via the RS232 interface to the host computer to enable the tag ID to be displayed. If a bit error is detected at step S19 then an error signal is generated at step S20 by the microprocessor and an error message displayed on the display 63.

If the answer at step S15 is no, the microprocessor then carries out steps S12 and S14 again to see if the

received data signal has been analysed for all known types of tags or transponders and if not to determine whether the maximum time T_0 allowed for the identification process has been exceeded. Again, if the answer to either of those questions is yes, the microprocessor proceeds to step S13. If the answer to both questions is no, then the microprocessor proceeds to analyse the incoming data stream in accordance with the modulation and data transmission system of the next known type of tag or transponder stored in the memory of the microprocessor. Again, the microprocessor 21 may adjust the selection of RF coil or coils where the antenna 26 comprises a microprocessor selectable RF coil arrangement. In this example, as shown in Figure 12c, the microprocessor 21 then checks to see if the transponder or tag is an EM Microelectronic Marin SA tag in which a 180° PSK rather than ASK modulation is used. Thus, the microprocessor controls the DSP2 at step S21 to provide PSK demodulated binary data. The microprocessor then carries out the same steps as S4 to S11 in Figure 12a and, if the tag or transponder is correctly identified as a PSK modulated tag or transponder produced by EM Microelectronic Marin SA, the decoded data is supplied to the host computer to enable the ID to be displayed. Again, if the answer at step S4 is no, the microprocessor repeats steps S12 and S14 to determine whether the incoming data stream has been

analysed according to the characteristics of all tags or transponders known to the microprocessor and, if not, whether the maximum time limit set for the interrogation has been exceeded. If the answer is in both cases no, the microprocessor assumes, in this example, that the tag or transponder is of the TIRIS family produced by Texas Instruments and supplies the 125kHz signal to the tag or transponder for the time known from the information stored in its memory to be required to charge the TIRIS tag, that is for a period of up to 50 milliseconds, at step S24. Again, where a microprocessor selectable RF coil arrangement is provided for the antenna, the microprocessor 21 may adjust the RF coil selection top optimise communication with the Texas TIRIS tag family. After a period of 50 milliseconds has expired, the microprocessor 21 controls the DSP2 to cause the incoming in-phase and quadrature data carrying signals to be processed as if they were FSK modulated in accordance with the TIRIS modulation and data transmission system. The FSK demodulation may be carried out at step S25 either by the filtering method described above with reference to Figure 9 in which, effectively, one of the in-phase or quadrature out-of-phase data carrying signals is filtered so as to pass only signals at the two modulation frequencies of the TIRIS tag or transponder or by using the comparison process described with reference to Figure 8. The microprocessor then checks

at step S26 to see if a valid FSK demodulated bit of the TIRIS data format has been received. If the answer is yes, the microprocessor stores the received bit at step S27. Steps S26 and S27 are repeated until the microprocessor determines at step S28 that 128 bits have been received. Once this is the case, the microprocessor checks to see if the received data contains any error in accordance with the error determining protocol of the TIRIS tag or transponder modulation and coding system. If the answer is yes at step S29, the microprocessor outputs an error message at step S30 to be displayed on the LCD of the host computer. If the answer is no at step S29, the microprocessor determines at step S31 that the tag or transponder is indeed a TIRIS type tag or transponder and transmits the decoded identification to the host computer.

If the answer at step S26 is no, the microprocessor may optionally change the interrogation frequency at step S32 by controlling the output frequency of the NCO 22. In particular, although it should be possible to charge a TIRIS tag or transponder using a 125kHz RF signal, the RF signal may be changed to the optimum charging frequency for the TIRIS tag system, namely 134.2kHz. Also, in this example, the microprocessor may control the clock extraction circuit 51, if provided, to enable extraction of the clock frequencies from the data carrying signals I and Q. Once the frequency has been

changed at step S32, the microprocessor waits for 50 milliseconds at step S32a to ensure that the tag or transponder is charged and then instructs the DSP2 to carry out the FSK demodulating procedure as discussed above at step S33. If the microprocessor determines that a valid FSK bit has been received at step S34, the process proceeds to step S27 and continues as discussed above. If, however, the microprocessor does not detect an FSK bit at step S34, steps S12 and S14 are again carried out. If the microprocessor determines that either all known types of tag have been checked for or the maximum time limit allowed for the interrogation has been exceeded, then the microprocessor determines that the interrogation is at an end at step S13 and supplies data to the host computer indicating that the tag cannot be identified. If the answers at steps S12 and S14 are no, the microprocessor 21 then proceeds to check for the next type of tag, in this example the IDESCO MICROLOG type of tag or transponder. Thus, the microprocessor 21 controls the NCO 22 to cause the antenna 26 to transmit the exciter pulses for the charging time known from the information stored in its memory to be required by the IDESCO tag or transponder at step S35. Again, the microprocessor 21 may adjust the RF coil selection to optimise communication between the antenna 26 and the tag 1 where the antenna comprises a microprocessor-selectable RF coil arrangement. Once the maximum required charging

time has expired, the microprocessor looks for a response to the exciter pulses (RSB) as described above with reference to Figure 5, as indicated by step S36 in Figure 12e. The DSP2 processes the in-phase and quadrature phase data carrier signals I and Q as if they were FSK modulated. If the DSP2 operates in the manner described above with reference to Figure 9, then the microprocessor controls the DSP2 to adjust the band-pass frequencies of the filters F3 and F4 to the two modulation frequencies used by the IDESCO modulation and coding system. The microprocessor then checks at step S37 whether a valid bit has been received. If the answer is yes, the bit is stored at step S38 and steps S37 and S38 repeated until the microprocessor determines at step S39 that all the bits known to be required for the IDESCO identification have been received. The microprocessor then checks at step S40 to see if there is any error in the received data in accordance with the IDESCO error checking procedure. If so, the microprocessor supplies a signal at step S41 to the host computer to indicate that the ID is invalid. If no error is detected, then the microprocessor determines at step S42 that the ID has been identified and supplies the ID to the host computer for display on the LCD display.

Although not shown in Figure 12e, if the microprocessor determines at step S37 that a valid bit has not been received, optionally the microprocessor may

operate the switch SW1 to prevent transmission of any RF signal between the exciter pulses and then control the NCO 22 to provide a substitute carrier frequency for the scaler 23 which is intermediate to the two modulation frequencies of the IDESCO tag and then instruct and DSP2 to repeat the FSK data processing routine.

If the answer at step S37 is no even after the above optional steps have been carried out, the microprocessor again carries out steps S12 and S14. If the answer at both steps S12 and S14 is no, then the microprocessor will proceed to analyse the incoming data for characteristics unique to the next type of tag stored in its memory. Alternatively, if the answer at either of steps S12 and S14 is yes, then the microprocessor sends a signal to the host computer indicating that the identification process has ended without the tag being identified and, if the user does not instruct the host computer that another tag is to be checked within a predetermined time limit, the microprocessor will power down the apparatus.

Of course, the order in which the apparatus checks for the various different types of tags or transponders may be now modified as desired.

Although particular examples of existing available transponders or tags have been described above, it should be appreciated that the present invention can be applied to any commercially available transponders or tags using

ASK or 180° PSK and responsive to an RF frequency within the range available to the apparatus which may be, for example, from 50 to 250kHz, depending upon the characteristics of the NCO 22 and possibly also of the antenna 26, although the use of a microprocessor-controllable RF coil arrangement would increase the flexibility of the apparatus. In addition, if the FSK data processing routine shown in Figure 8 is used, then tags or transponders using FSK modulation with different frequencies from those described above may also be identified. Of course, if the band-pass of the filtering in the example shown in Figure 9 can be controlled by the microprocessor, then the filtering processing could also be used to analyse for FSK modulation schemes using other frequencies. Also, the PSK demodulation process may be adaptable to other PSK modulation schemes. Similarly, by reprogramming the DSPs in the apparatus shown in Figure 6, other modulation schemes may be accommodated as and when their use becomes known, for example, QPSK or spread spectrum modulation schemes may be incorporated. In addition, other methods for trying to identify a particular tag may be used. For example, a digital signal processor may be programmed to carry out a Fast Fourier Transform (FFT) on the response signal from the transponder 1 and the microprocessor 21 may then compare the resulting spectrum with stored data, for example the microprocessor 21 may be provided with a look

up table containing information on characteristic features of the spectrum of different tags or transponders 1 and may then compare the FFT spectrum from the DSP with the information in the look up table to identify the particular tag, so as to enable its data to be decoded, if necessary, and retrieved.

It should be appreciated that the above described types of tags or transponders are only examples and that the present invention could also be applied to other types of tags with different modulation and data transmission systems provided that the microprocessor has access to the information necessary to enable characteristic features of a tag's modulation and data transmission system, for example characteristic features of its data format, to be identified and the identified tag then to be read. As new types of tag or transponder become known the programming of the DSPs, the microprocessor and the information stored in memory may be changed or updated by coupling the apparatus to a host computer. Updating may even, for example, be carried out by a user installing updated software and information supplied on a suitable data carrier by the supplier of the apparatus via a host computer coupled to the apparatus. The digital signal processors may, where necessary, be modified to cope with different carrier modulation and data transmission systems as these arise. It may also be possible for the apparatus microprocessor

to have access to information regarding common carrier modulation techniques and data format/coding systems not currently used for tags or transponders to allow the apparatus to attempt to read an unknown tag by using its information regarding commonly known carrier modulation techniques and format/coding systems.

Although in the examples described above, digital signal processors have been used to increase the speed with which a tag can be read, where speed is not essential or when faster more powerful microprocessors become available, it may be possible to replace the digital signal processors with microprocessors to facilitate modification of the processing operations.

Although the above description has been directed to passive data storage tags in the form of low radio frequency identification tags or transponders, it should be appreciated that the present invention may be applied to, for example, passive data storage tags which operate at other electromagnetic frequencies, for example frequencies in the Megahertz and Gigahertz (for example 2.45GHz) ranges and including microwave frequencies, with appropriate modification of the antenna structure and operating frequencies. It may also be possible to apply the present invention to passive data storage devices where activation and data transmission is carried out by some form of opto-electronic coupling. In addition, the present invention could be applied to remotely readable

data storage devices such as so-called active tags which have some form of internal power source, for example a battery backed up RAM.

Also, once the data storage device has been identified as described above apparatus embodying the present invention may be used to enable data to be written to a data storage device where the data storage device is designed to allow data to be written to the device.

Other modifications and variations will be apparent to those skilled in the art.

CLAIMS:

1. Apparatus for remotely reading data from a number of different manufacturer's data storage devices such as radio frequency identification transponders, which apparatus comprises means for determining the modulation system used by such a data storage device to transmit data and for checking for features characteristic of the data transmission system of a particular manufacturer's data storage devices in a response signal transmitted by the data storage device to the apparatus and means for analysing the response signal in accordance with the identified features to determine the data stored by the data storage device.

2. Apparatus for remotely reading data from a number of data storage devices each designed to communicate data to a corresponding compatible reader in response to an interrogation signal from that reader and using a carrier modulation and data transmission system designed for that data storage device and corresponding reader, the apparatus comprising means for storing information relating to different possible carrier modulation and data transmission systems, means for interrogating a data storage device by transmitting a signal to the data storage device, means for receiving a response signal from the data storage device, means for determining using

information stored by the storing means and the response signal the particular carrier modulation and data transmission system of the data storage device, and means for analysing the response signal in accordance with the identified carrier modulation and data transmission system to determine the data stored by the data storage device.

3. Apparatus according to claim 1 or 2, wherein the determining means comprises means for identifying whether the response signal uses any one of a number of different types of carrier modulation systems.

4. Apparatus according to claim 3, wherein the identifying means comprises means for processing the response signal as if it were using a given one of the different modulation systems to produce a processed signal, means for deciding from the processed signal whether the response signal used that modulation system and means for causing the processing means to repeat the processing for another of the different modulation systems if the deciding means decides that modulation system was not used.

5. Apparatus according to claim 4, wherein the processing means comprises a digital signal processor.

6. Apparatus according to claim 4 or 5, wherein the deciding means comprises a microprocessor.

7. Apparatus according to claim 4, 5 or 6, wherein the deciding means comprises means for checking whether the processed signal represents a binary data stream of one of the possible carrier modulation and data transmission systems.

8. Apparatus according to claim 7, wherein the deciding means comprises means for decoding the processed signal in accordance with a coding system used by one of the possible different carrier modulation and data transmission systems having the given modulation scheme.

9. Apparatus according to any one of claims 4 to 8, wherein the deciding means comprises data format comparison means for comparing the processed signal with information stored by the storing means relating to possible data format systems of the different possible carrier modulation and data transmission systems to determine whether the processed signal has a valid data format.

10. Apparatus according to any one of claims 4 to 9, wherein the identifying means comprises means for mixing a response signal received by the receiving means with

an in-phase carrier signal and with a quadrature out-of-phase carrier signal to provide in-phase and quadrature out-of-phase data carrying signals.

11. Apparatus according to claim 10, further comprising analog-to-digital conversion means for converting the response signal to a digital response signal and wherein the generating means are adapted to provide binary in-phase carrier and quadrature out-of-phase carrier signals for mixing with the digital response signal.

12. Apparatus according to claim 10 or 11, wherein the identifying means comprises means for filtering the in-phase and quadrature out-of-phase data carrying signals to remove the carrier signal.

13. Apparatus according to any one of claims 10 to 12, wherein the identifying means comprises means for comparing one of the in-phase and quadrature out-of-phase signals with an average over time of the one of the in-phase and quadrature out-of-phase signals to provide an amplitude modulation demodulated output signal to the deciding means.

14. Apparatus according to any one of claims 10 to 13, wherein the identifying means comprises means for supplying the waveform of the quadrature out-of-phase

data carrying signal to the deciding means.

15. Apparatus according to any one of claims 10 to 14, wherein the identifying means comprises first and second band pass filtering means for each filtering one of the in-phase and quadrature out-of-phase signals and supplying an output signal to the deciding means.

16. Apparatus according to any one of claims 10 to 15, wherein the identifying means comprises comparing means for providing outputs dependent on the change of amplitude of the in-phase and quadrature out-of-phase signals with time to the deciding means.

17. Apparatus according to any one of the preceding claims, further comprising control means for causing, when the determining means determines that no response signal has been received by the receiving means, the transmitting means to send a signal for a predetermined period to charge the data storage device and for causing the determining means to determine whether a response signal has been received at the end of the predetermined period.

18. Apparatus according to claim 17, wherein the control means is adapted to change the frequency of the transmission means if no response is received at the end

of the predetermined period and then to cause the determining means to determine whether a response signal is received within another predetermined period.

19. Apparatus according to claim 17 or 18, wherein, when no response is received within the predetermined or a further predetermined period, the control means causes the transmitting means to generate periodic excitor signal bursts and causes the determining means to determine whether a response signal is received in response to an excitor signal burst.

20. Apparatus according to any one of the preceding claims, wherein the apparatus is housed within a hand-holdable casing.

21. Apparatus according to any one of the preceding claims, further comprising a communications interface for communicating with a host computer.

22. Apparatus according to any one of the preceding claims, further comprising means for reading bar codes.

23. Apparatus according to any one of the preceding claims, further comprising means for modifying the signal transmitted to the data storage device.

24. Apparatus according to any one of claims 1 to 22 adapted to read data remotely from radio frequency identification tags or transponders.

25. Apparatus according to claim 24, wherein the transmitting means comprises an RF coil arrangement and means for selecting an RF coil or coil combination.

26. A method for remotely reading data from a number of different manufacturer's data storage devices such as radio frequency identification transponders, which method comprises determining the modulation system used by such a data storage device to transmit data and checking for features characteristic of the data transmission system of a particular manufacturer's data storage devices in a response signal transmitted by the data storage device to the apparatus and analysing the response signal in accordance with the identified features to determine the data stored by the data storage device.

27. A method for remotely reading data from a number of data storage devices each designed to communicate data to a corresponding compatible reader in response to an interrogation signal from that reader and using a carrier modulation and data transmission system designed for that data storage device and corresponding reader, the method comprising storing information relating to different

possible carrier modulation and data transmission systems, interrogating a data storage device by transmitting a signal to the data storage device, receiving a response signal from the data storage device, determining using stored information and the response signal the particular carrier modulation and data transmission system of the data storage device, and analysing the response signal in accordance with the identified carrier modulation and data transmission system to determine the data stored by the data storage device.

28. A method according to claim 26 or 27, which comprises identifying whether the response signal uses any one of a number different types of carrier modulation systems.

29. A method according to claim 28, which comprises identifying the modulation system by processing the response signal as if it were using a given one of the different modulation systems to produce a processed signal, deciding from the processed signal whether the response signal used that modulation system and repeating the processing for another of the different modulation systems if that modulation system was not used.

30. A method according to claim 29, wherein the deciding step comprises checking whether the processed signal represents a binary data stream of one of the possible carrier modulation and data transmission systems.

31. A method according to claim 30, wherein the deciding step comprises decoding the processed signal in accordance with a coding system used by one of the possible different carrier modulation and data transmission system having the given modulation scheme.

32. A method according to any one of claims 29 to 31, wherein the deciding step comprises comparing the processed signal with information stored by the storing means relating to possible data format systems of the different possible carrier modulation and data transmission systems to determine whether the processed signal has a valid data format.

33. A method according to any one of claims 26 to 32, which comprises, when no response is received within a predetermined period, continuing transmission of a signal to the data storage device for a predetermined time to charge the device and then determining whether a response is received.

34. A method according to claim 33, which comprises, after the predetermined period, if no response signal is received, generating periodic excitor signal bursts and determining whether a response signal is received in response to an excitor signal burst.

35. A method according to any one of claims 26 to 32 for reading data remotely from radio frequency identification tags or transponders.

36. Apparatus for remotely reading data from a number of data storage devices substantially as hereinbefore described with reference to the accompanying drawings.

37. A method for remotely reading data from a number of data storage devices substantially as hereinbefore described.

Patents Act 1977 54 **Examiner's report to the Comptroller under Section 17 (The Search report)**	Application number GB 9517792.9
Relevant Technical Fields (i) UK Cl (Ed.N) G4H (HNLB, HNNC); H4L (LACA, LASS) (ii) Int Cl (Ed.6) G01S 13/02, 13/76, 13/82; G06K 7/00, 7/08, 7/10	Search Examiner MR N HALL Date of completion of Search 4 DECEMBER 1995
Databases (see below) (i) UK Patent Office collections of GB, EP, WO and US patent specifications. (ii) ONLINE: WPI	Documents considered relevant following a search in respect of Claims :- 1-37

Categories of documents

X: Document indicating lack of novelty or of inventive step.

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A: Document indicating technological background and/or state of the art.

P: Document published on or after the declared priority date but before the filing date of the present application.

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&: Member of the same patent family; corresponding document.

Category	Identity of document and relevant passages		Relevant to claim(s)
X	GB 2268664 A	(PLESSEY) see whole document	1, 2, 26, 27 at least
X	EP 0583526 A1	(THOMSON) see whole document	1, 2, 26, 27 at least
X	EP 0565469 A1	(INNOVATRON) see whole document	1, 2, 26, 27 at least
X	EP 0554164 A1	(GEMPLUS) see whole document	1, 2, 26, 27 at least
X	EP 0513507 A1	(TOSHIBA) see whole document	1, 2, 26, 27 at least
X	EP 0498678 A2	(FUJITSU) see whole document	1, 2, 22, 26, 27 at least
X	EP 0494710 A2	(GREEN BIT) see whole document	1, 2, 26, 27 at least
X	US 5420412	(KOWALSKI) see whole document	1, 2, 26, 27 at least

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Category	Identity of document and relevant passages	Relevant to claim(s)
X	US 5329104 (ALPS) see whole documet	1, 2, 22, 26, 27 at least